Sanjay Patel

Architect/Engineer/Inventor

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EXPERIENCE

Performance Architect Apple Computer Cupertino, California	**Co-authored software performance tools suite.** Developed system-wide profiler (Shark - http://developer.apple.com/tools/sharkoptimize.html), instruction trace analyzer, CPU core benchmarks, memory system benchmarks, CPU power/heat generator. Created code analysis engine in profiler to annotate software with optimization hints. Led design of human interfaces for all applications. **Managed and led marketing of performance tools.** Set product design goals and schedules. Demonstrated tools internationally including four years at Apple Worldwide Developer Conference. Held "Code Kitchens." Created and staffed feedback forums. Responsible for bug and feature database management. **Analyzed and optimized performance critical code for software teams.** Worked with Apple Applications (iTunes, Quicktime, Final Cut Pro, Shake, Keynote, Soundtrack), Mac OS kernel/libraries, Adobe (Photoshop, Illustrator, After Effects, Acrobat), Id/Aspyr (Quake, Doom), Alias Maya, Maxon Cinema4D, Pixar Renderman, NewTek Lightwave, and many others. **Drove CPU architecture and implementation.** Collaborated with Intel, IBM, and Freescale on micro-architecture and designs for G3, G4, G5, and future CPUs. Brought hard data and vision to hardware design efforts. **Guided compiler optimization efforts.** Combined assembly language (PPC, x86) and CPU expertise to help GCC, ICC, XLC, and CodeWarrior compiler teams. Improved compiler codegen for several micro-architectures. **Measured and projected performance of current and future Macintosh systems**. Evaluated hardware and software design trade-offs. Developed fully automated system performance benchmarks. **Received highest employee evaluation for seven consecutive years.** Promoted twice within Apple engineering rankings, applied for two patents, and earned several awards.	1998–2006

EXPERIENCE		
Engineering Intern IBM Austin, TX	Worked on design verification of POWER3 and POWER4 CPUs. Developed simulation models of the instruction sequencing unit and caches. Tutored co-workers in C++ design. Developed stand-alone assembly-level test generation program and its run-time environment.	1997–1998
Teaching Assistant UC Berkeley Berkeley, CA	Led discussion sections of introductory electrical engineering class for computer science students, defined sample problems, handled student questions, and assisted grading exams.	1997–1998
Engineering Intern Intel Hillsboro, OR	Designed RTL models of L2 caches and verified functional equivalency of schematics and models. Used Intel tools for RTL entry and compilation, vector-based validation, and formal verification.	1997
Engineering Intern AMD Austin, TX	Performed board-level design, test, and debug for an InterWave-based sound card for PCs. Designed CD-ROM and local memory interfaces and developed the InterWave Effects Tool software application. Assisted with design verification on the AMD K5 CPU.	1994-1996

COMPUTER SKILLS	
Systems	Mac OS X, Linux/UNIX, Windows, Amiga
Languages	C/C++, SIMD programming (AltiVec, MMX, SSE), Assembly (PowerPC, x86), Objective C, Java, Fortran, English
Applications	Xcode, GCC, GDB, ICC, XLC, CodeWarrior, MS Visual Studio, MS Office, Shark

EDUCATION			
Entrepreneur's Bootcamp	Syracuse University Syracuse, NY	Six week crash course in business, marketing, finance, accounting, operations, planning	2005
Master of Science Electrical Engineering (thesis pending)	University of California Berkeley, CA	Research: Computer Aided Design GPA: 3.9/4.0	1997-1998
Bachelor of Science Electrical and Computer Engineering	University of Texas Austin, TX	Graduated Magna Cum Laude GPA: 3.9/4.0	1992-1996

OTHER
U.S. citizen, world traveler, painter, poker player, National Merit Finalist References available upon request